IN THE CLAIMS

Please cancel claims 1-13 and 19-20 without prejudice.

Please amend claim 15 as follows below.

Please add new claims 21-29 that follow below.

MARKED UP VERSION OF PENDING CLAIMS

1-13. (Cancelled)

14. (Original) An instruction set architecture (ISA) for execution of operations within a digital signal processor, the instruction set architecture comprising:

a set of instructions for operation within a digital signal processor wherein each instruction includes a first operand accessed directly from memory, a second operand accessed directly from memory of a local register, and a destination register to store results, the set of instructions including,

a 20-bit DSP instruction, and

a 40-bit DSP instruction,

the set of instructions to accelerate calculations within the digital signal processor of

the type where D = [(A operation one B) operation two C] where operation one and operation two are separate signal processing operations.

15. (Currently Amended) The instruction set architecture (ISA) of claim 14 for execution of operations within a digital signal processor, wherein,

the twenty bit instruction uses mode bits in control registers (i.e. mode registers) and the forty bit instruction has a control extension to override the mode bits ~~registers~~.

16. (Original) The instruction set architecture (ISA) of claim 14 for execution of operations within a digital signal processor, wherein,

the set of instructions further includes a dyadic instruction to execute two operations in one instruction.

17. (Original) The instruction set architecture (ISA) of claim 16 for execution of operations within a digital signal processor, wherein

the two operations of the dyadic instruction for execution in one instruction are DSP operations.

18. (Original) The instruction set architecture (ISA) of

claim 17 for execution of operations within a digital signal processor, wherein

the DSP operations are of the set of operations of multiplication, addition, extremum, and no operation.

19-20. (Cancelled)

21. (New) The instruction set architecture (ISA) of claim 15 for execution of operations within a digital signal processor, wherein,

the control registers are mode registers.

22. (New) An instruction set architecture of an application specific signal processor to convert voice and data samples into packets for transmission over a network and to convert packets received from the network into voice and data samples, the instruction set architecture comprising:

a DSP instruction set architecture for a plurality of signal processing units to control the datapaths thereto and execute DSP operations therein;

and

a control instruction set architecture for a RISC control unit to control the execution of DSP instructions by the plurality of signal processing units.

23. (New) The instruction set architecture of claim 22, wherein

the DSP instruction set architecture includes

a 20-bit DSP instruction, and

a 40-bit DSP instruction.

24. (New) The instruction set architecture of claim 23, wherein

the 20-bit DSP instruction uses mode bits in mode registers to further control instruction execution.

25. (New) The instruction set architecture of claim 24, wherein

the 40-bit DSP instruction has a control extension to override the mode bits in the mode registers.

26. (New) The instruction set architecture of claim 23, wherein

the DSP instruction set architecture further includes a 20-bit dyadic DSP instruction, and

a 40-bit dyadic DSP instruction.

27. (New) The instruction set architecture of claim 23,

wherein

the control instruction set architecture for the RISC control unit includes

a 20-bit control instruction, and

a 40-bit control instruction.

28. (New) An instruction set architecture of an application specific signal processor to convert voice and data samples into packets for transmission over a network and to convert packets received from the network into voice and data samples, the instruction set architecture comprising:

a digital signal processing (DSP) instruction set architecture for a plurality of signal processing units to control the datapaths thereto and execute DSP operations therein, the DSP instruction set architecture including

a 20-bit DSP instruction,

a 40-bit DSP instruction,

a 20-bit dyadic DSP instruction,

a 40-bit dyadic DSP instruction, and

wherein the 20-bit dyadic DSP instruction and the 40-bit dyadic DSP instruction include a main digital signal processing operation and a digital signal processing operation;

and

a control instruction set architecture for a RISC control unit to control the execution of DSP instructions by the plurality of signal processing units.

29. (New) The instruction set architecture of claim 28, wherein

the digital signal processing operations are of the set of operations of multiplication, addition, extremum, and no operation.